

Image



2829

IN THE UNITED STATES
PATENT AND TRADEMARK OFFICE

PATENT APPLICATION

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CASE: S1

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EXAMINER: Nguyen, Vinh P

TITLE: TESTING INTEGRATED CIRCUITS

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In response to the Office Action mailed 01/06/04 please amend the above-identified application as follows, and consider the remarks that follow the amendments.

Please change the title to read:

-- MEMBRANE TEST METHOD AND APPARATUS FOR
INTEGRATED CIRCUIT TESTING --

Please amend the paragraph beginning at line 6 on page 12 as follows:

An even more effective arrangement for reducing the electrical path of the test vectors is shown in Fig. 5. Here the reference circuit is divided, with some components located directly on the sidewalls of the probe membrane, and other components located as in Fig. 3. The figure shows inductors 44 and capacitors 45 mounted on the sidewalls of the membrane as shown. These passive circuit elements are representative of components that may be selected for optimized test signal length. Other circuit elements may be chosen for this location. In this embodiment the IC reference chip 32 for the overall system is shown mounted according to the embodiment of Figs. 3 and 4, with only selected device components removed to the sidewall of the membrane. The reference L,C elements 44, 45 are shown as separate elements for illustration but may be integrated on a silicon or ceramic chip. The chip may then contain all of the elements necessary for matching the I/Os of the chip under test. Several chips, e.g. four chips one on each side of the pyramid, may contain the impedance matching elements for each of four rows of I/Os on the chip under test. The elements integrated on the silicon or ceramic chip may ~~comprises~~ comprise just L and/or C elements, which is referred to herein as a passive IC chip, or may comprise active elements such as transistors, and is referred to here and below as an active IC chip. The term IC chip may refer to either or both.